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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,421	07/18/2003	Chih-Yuan Wang	MR1683-479	2796

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,421	WANG ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 1, item 131 and Figure 5, item 831. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory

obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-4 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5 of copending Application No. 10/731,017. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending claims are the broader version of the present claims.

The following is an example for comparing claim 1 of this application and claim 1 of copending Application No. 10/731,017.

Claim 1 of this application	Claim 1 of Application No. 11/731,017
A damping and muffling structure for EL cell, comprising	A damping and muffling structure for EL cell, comprising
a transparent substrate, a front electrode layer, a lighting layer and an insulating layer for packaging the EL cell,	a transparent substrate, a front electrode layer, a lighting layer, **an inducing layer, a back electrode layer** and an insulating layer for packaging the EL cell,
the front electrode layer, lighting layer and insulating layer being sequentially overlaid on the substrate, **an inducing layer** and at least one conductive layer being laid on	the front electrode layer, lighting layer, **inducing layer, back electrode layer** and insulating layer being sequentially overlaid on the substrate,

the lighting layer, **a back electrode layer being laid on the inducing layer, the conductive layer being laid on the lighting layer in such a position as not to affect light emitting of the lighting region,**	
the conductive layer being also laid on at least one side between both the lighting layer and the inducing layer **and connected with the back electrode layer**,	a conductive layer being laid between the lighting layer and the inducing layer, **the conductive layer being connected to the grounding electrode**
the front and back electrode layers being connected with a driving circuit,	the front and back electrode layers and the conductive layer being connected to a driving circuit having a grounding electrode
the back electrode layer being connected to a grounding electrode of the driving circuit,	
whereby the conductive layer can conduct the charge accumulating on the inducing layer.	whereby the conductive layer can conduct the charge accumulating on the inducing layer to the grounding electrode.

As can bee seen from above, the first difference between claim 1 of this application and claim 1 of the copending application is that the present application recites of "the conductive layer being laid on the lighting layer in such a position as not to affect light emitting of the lighting region" which is not recited in the copending application, however, it is inherent that the conductive layer would be positioned as to not affect the light emitting region.

The second difference between claim 1 of this application and claim 1 of the copending application is that the copending application recites of "the front electrode layer, lighting layer, inducing layer, back electrode layer and insulating layer being sequentially overlaid on the substrate" whereas the present invention recites of "the front electrode layer, lighting layer and insulating layer being sequentially overlaid on

the substrate" and then follows with reciting that the inducing layer is laid on the lighting layer an the back electrode layer is laid on the inducing layer, which results in the two structures being equivalent.

The third difference between claim 1 of this application and claim 1 of the copending application is that the present application recites of the conductive layer being connected to the back electrode and the back electrode being connected to a grounding electrode of the riving circuit, whereas the copending application recites of the conductive layer being connected to the grounding electrode, and since the claims are in comprising format, the present claims are not patentably distinct from the copending claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimaki et al. (JP 11273872 A) in view of Wachi et al. (US 2003/0085649).

Regarding claim 1, Nishimaki et al. disclose a damping and muffling structure for EL cell (Drawing 1), comprising

a transparent substrate (Drawing 1, 2a and paragraph [0008[),

a front electrode layer (Drawing 1, 3a and paragraph [0008]),

a lighting layer (drawing 1, 4 and paragraph [0008]) and

an insulating layer for packaging the EL cell (drawing 1, 2b and paragraph [0008]),

the front electrode layer, lighting layer and insulating layer being sequentially overlaid on the substrate (Drawing 1),

an inducing layer (Drawing 1, 5 and paragraph [0008]. The examiner interprets that a dielectric layer is an inducing layer.) and at least one conductive layer (Drawing 1, 8a) being laid on the lighting layer (Drawing 1. Dielectric layer 5 is laid on the lighting

layer 4 and the conduction film 8a is laid on layer 7, which is laid on layer 6a, which is laid on layer 5, which is laid on the lighting layer 4.),

a back electrode layer (Drawing 1, 6a) being laid on the inducing layer (Drawing 1. Back plate 6a is laid on dielectric layer, the inducing layer, 5),

the conductive layer being laid on the lighting layer in such a position as not to affect light emitting of the lighting region (It is inherent that the conductive layer would be laid such as to not affect light emitting of the lighting region.),

the front and back electrode layers being connected with a driving circuit (Drawing 1, back plate 6a and front electrode 3a are connected to driving circuit 10.).

The first embodiment of Nishimaki et al. fails to teach of a damping and muffling structure for EL cell comprising

the conductive layer being connected with the back electrode layer and the back electrode layer being connected to a grounding electrode of the driving circuit.

The second embodiment of Nishimaki et al. discloses of a damping and muffling structure for EL cell comprising the conductive layer (Drawing 2, 13) being connected with the back electrode layer (Drawing 2, 15) and the back electrode layer (Drawing 2, 6a) being connected to a grounding electrode of the driving circuit (Drawing 2, 9a).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to combine the first and second embodiments taught by Nishimaki et al. such that the structure of the first embodiment would be preserved, however, the conductive layer would be connected to the back electrode, which in turn

would be connected to the ground electrode of the driving circuit as in the second embodiment, in order to effectively reduce the noise being generated by the EL cell.

The two embodiments of Nishimaki et al. fail to teach of the conductive layer being also laid on at least one side between both the lighting layer and the inducing layer whereby the conductive layer can conduct the charge accumulating on the inducing layer.

Wachi et al. disclose of a conductive layer (Figure 3, 15) being also laid on at least one side between both a lighting layer (Figure 3, 2. The examiner interprets that the display panel main body 2 would contain a lighting layer to light the display.) and an inducing layer (Figure 3, 14 and paragraph [0063]. The examiner interprets that given the transparent substrate's heat buffering function that it would constitute as an inducing layer.) whereby the conductive layer can conduct the charge accumulating on the inducing layer (The examiner interprets that since conductive layer 15 and substrate 14 are in contact that the conductive layer would be able to function to conduct charge formed on the substrate.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to place the conductive layer in-between the lighting layer and the inducing layer, as taught by Wachi et al., in the EL cell as taught by the embodiments of Nishimaki et al. in order to decrease electromagnetic noises generated from the display panel main body.

Regarding claim 2, Nishimaki et al. and Wachi et al. disclose the damping and muffling structure for EL cell as claimed in claim 1. Wachi et al. also disclose wherein the conductive layer is made of conductive material including inorganic metal, organic conductive material and organic/inorganic complex conductive material (Paragraphs [0043] and [0044]).

Regarding claim 3, Nishimaki et al. and Wachi et al. disclose the damping and muffling structure for EL cell as claimed in claim 1. The second embodiment of Nishimaki et al. also discloses

wherein the conductive layer is laid on the lighting layer on one side of the inducing layer without affecting the light emitting of the lighting region of the lighting layer (See discussion of claim 1),

the conductive layer being in contact with and electrically connected with the back electrode layer without contacting with the front electrode layer (Drawing 2, the conductive layer 13 contacts the back plate 6a through connection 15 without contacting the front electrode 3a since the substrate 2a is in-between the two.).

Wachi et al. does not explicitly teach of a conductive layer being also laid on the same side between an inducing layer and a back electrode layer, however, the display panel main body 2 of Figure 3 would have a back electrode layer, which would mean that the conductive layer 15 would be in-between the back electrode and the substrate, inducing layer, 14.

Regarding claim 4, Nishimaki et al. and Wachi et al. disclose the damping and muffling structure for EL cell as claimed in claim 1. Nishimaki et al. also discloses wherein the front and back electrode layers are respectively connected with two outward extending conductive terminals for connecting with the driving circuit (Drawing 1, 3b and 6b and paragraph [0008]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

18 November 2005

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER